

SYN1588[®] enabled IEEE 1588 compliant clock synchronization

SYN1588Clock_S IP Core

Brief Data Sheet

Version 1.2 – March 10th 2008

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0 Introduction

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0.1 Versions

Version 1.2 March 10th 2008

- Update of text and new features with respect to IEEE1588 version 2.0
- New graphics added

Version 1.1, June 28th 2007

- Update of new office address.

Version 1.0, February 24th 2006

- Created document.

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1 SYN1588Clock_S IP Core

1.1 Functional Description

The SYN1588[®]Clock_S IP-core provides highly accurate clock synchronization compliant to the IEEE 1588 standard version 1.0 and 2.0. It comprises a high resolution, high accuracy hardware clock which uses a 96-bit wide adder based clock architecture allowing supporting arbitrary input clock frequencies in the range of 10 – 200 MHz. Furthermore the SYN1588[®]Clock_S contains an MII-Scanner unit, responsible for scanning all Ethernet traffic in search for IEEE1588 synchronization packets. Upon detection of any such packet it draws a 96-bit wide time stamp from the local clock any copies it together with status and identification data of the packet into a so-called time-stamp FIFO. This FIFO in turn is processed by the PTP-stack.

In figure 1 the basic clock architecture used for all SYN1588[®] IP cores is shown. The clock contains an accumulator whose increment and current value is user adjustable without causing glitches or spikes in the output signal.

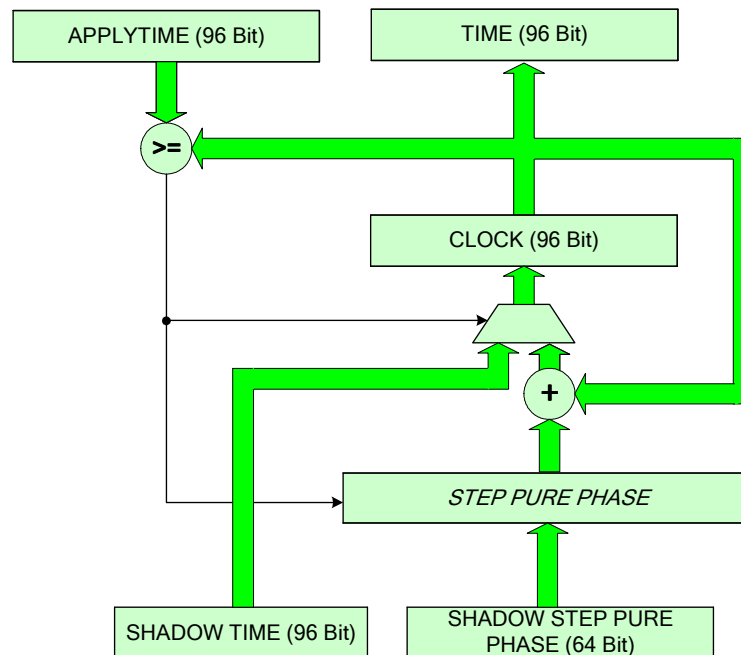


Figure 1: SYN1588Clock_S High Accuracy Clock Architecture.

For 10/100 Mbit/s designs, the core is connected to the system's Ethernet MII port (according to IEEE 802.3 clause 22) and an SPI port of the host processor of the node as shown in following figure 2.

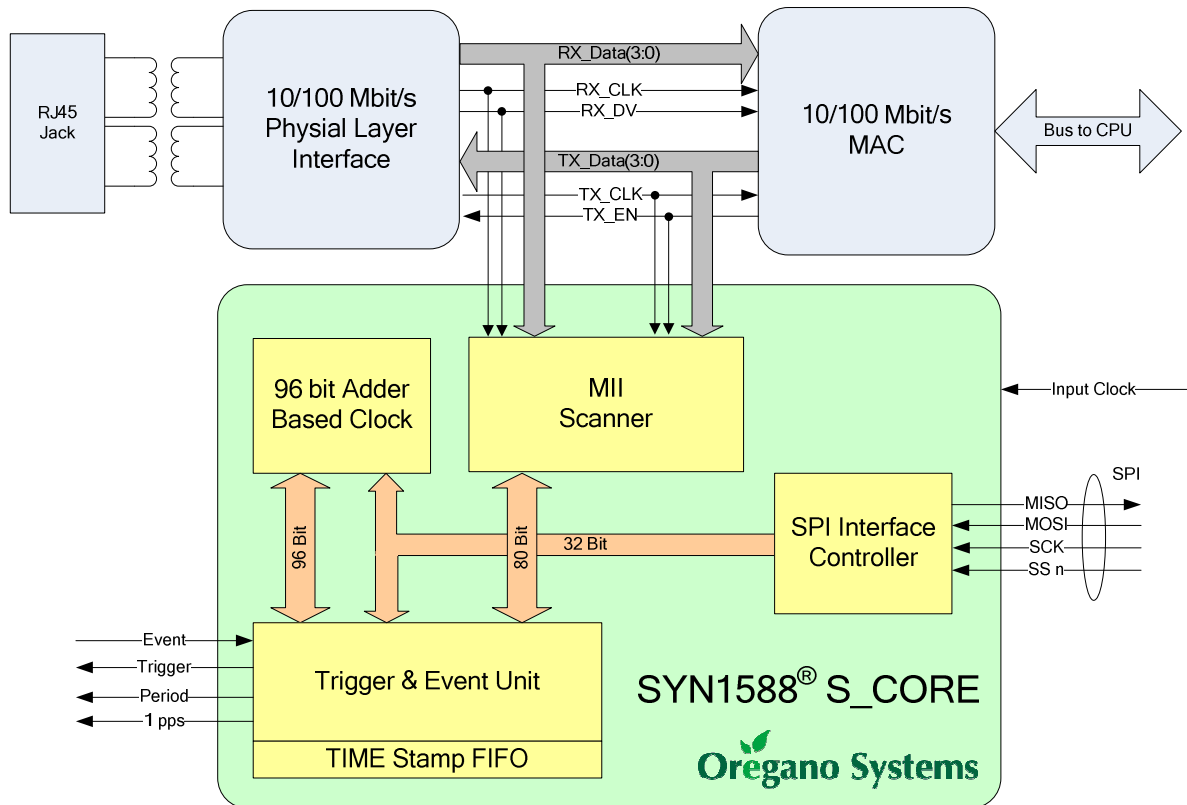


Figure 2: SYN1588Clock_S 10/100 Mbps block diagram.

The core supports Gbit/s Ethernet transmission rates as well via the GMII interface (following IEEE 802.3u clause 22.4), to which is has to be attached for such a solution as shown in figure 3. Please note that Oregano Systems supports other flavours of the MII upon request such as RMII. However, due to the inherent limitations of these interfaces with respect to clock synchronization Oregano Systems does not recommend their usage

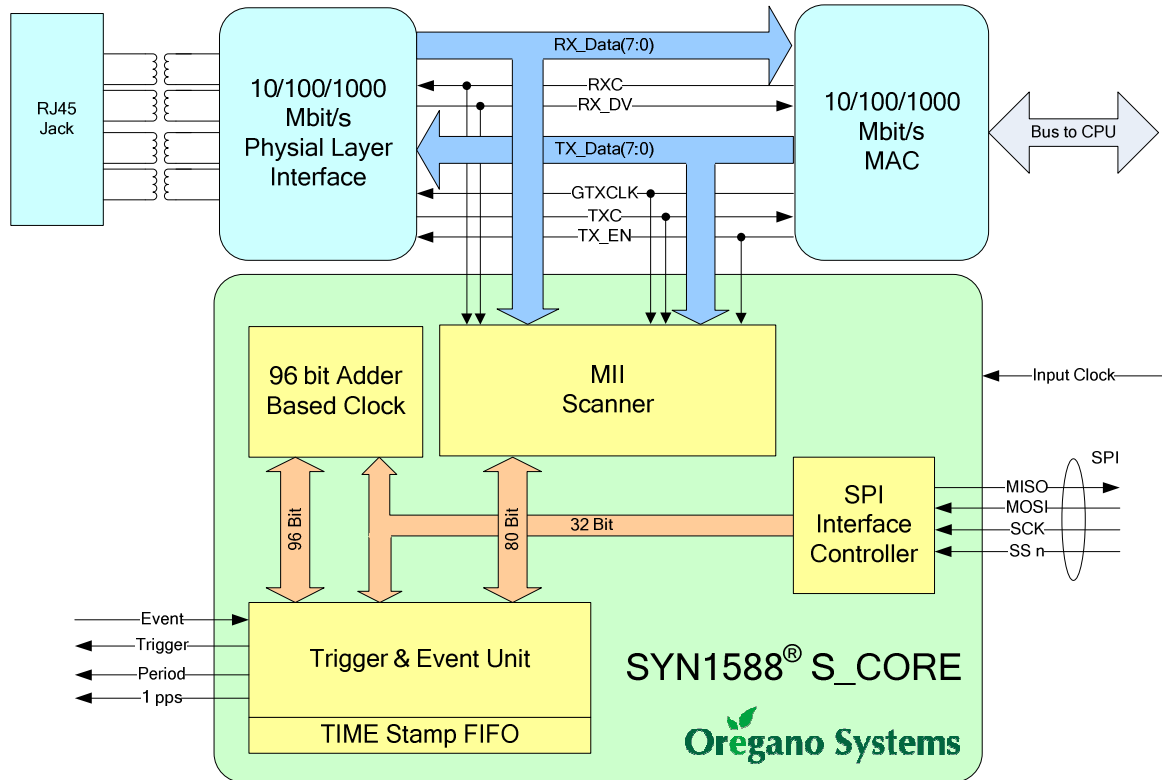


Figure 3: SYN1588Clock_S 1000 Mbps block diagram.

The Oregano System's SYN1588[®] Clock_S is intended to be used in embedded systems with stringent requirements on both space and costs. For example, it easily fits into the smallest members of both the LATTICE XP and XP2 families as a single chip addition to existing designs. A possible system block diagram is shown in figure 4.

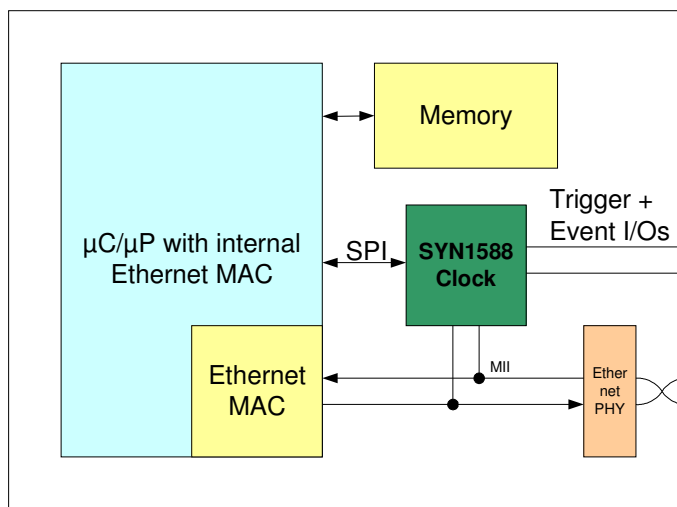


Figure 4: SYN1588Clock_S 1000 Mbps block diagram.

1.2 Features

Together with an appropriate IEEE 1588 compliant PTP-stack (also offered by Oregano Systems) the SYN1588[®]Clock_S will synchronize its local clock to a master. As a standard output of the IP core a 1 pps pulse is generated which is phase locked for all nodes synchronized to each other in a given network. If the SYN1588[®]Clock_S IP core is connected to an external time reference (e.g. a GPS based time source via a 1 pps input and a serial data line) the clock may lock to this pulse and act as an IEEE 1588 compliant master.

On application level the SYN1588[®]Clock_S offers one so-called event-input pin, which may be used to record signal transitions with the accuracy of the SYN1588[®] clock. Aside from the 1 pps output the IP core is able to generate an arbitrary frequency with a resolution of less than 0.1 Hz by means of the so-called period timer, which again is linked to the internal clock. Finally a trigger output allows generating a signal transition at a given point in time.

The features of the IP core are summarized as follows:

- Small footprint and small I/O count
- The core is completely synchronous to the system clock
- All registers of the core operate with the rising edge of the system clock
- The clock time format is compatible to the IEEE1588 standard version 2002 and 2008
- Supports 10/100 Mbit/s half & full duplex modes via MII
- Supports 10/100/1000 Mbit/s via GMII
- Supports SPI cascade and independent slave mode
- SPI data rates up to 20 Mbit/sec
- 16-bit SPI data transfers
- 32 bit interface to the internal SPI controller
- 1 pps output
- 1 period timer output allowing generating user configurable output frequencies with a period ranging from 14,000 sec down to 200 nsec with a resolution of 1 Hz.
- 1 event input which draws a time stamp and stores it in the time stamp FIFO upon polarity changes of the input pin. This input may be used to synchronize to an external GPS-based time source via a 1 pps signal
- Events may be processed at a burst rate of 1 MHz. The sustained event rate is dependent on the performance of the host processor.
- 1 trigger output signal which may be used to generate a signal transition at a given point in time
- All event, period, and trigger signals are strictly synchronous to the internal high accuracy clock.
- The time of the clock core is easily available via register accesses to the application software and so are the event, trigger, and period registers.
- Coded in VHDL
- Delivered with test bench, 100% code coverage guaranteed
- Support of GPS timing receivers
- Optional features available upon request
 - On-the-Fly time stamping
 - PTP Version 1.0 and version 2.0 stack (Linux or Windows[®])
 - RMII Interface
 - Enhanced MII scanner to be used to detect and subsequently time stamp a configurable type of Ethernet traffic both for send and receive data

- Variable clock rate adjusted (continuous amortization)
- SGMII and other serial interface options between MAC and physical layer IC
- Pipelined adder based clock to support various system clock signal frequencies

1.3 Resource utilization

The following table designates the resource utilization of an implementation of several of the most common FPGA families and devices. If you need further information on resource utilization for a specific FCPGA not listed please contact Oregano Systems.

For high accuracy and high speed applications Oregano Systems strongly recommends utilizing Xilinx devices.

DEVICE	Utilization	System Freq.
Lattice XP	1668 Slices, 1954 LUT4s, 4 EBRs	75 MHz
Lattice XP2	1552 Slices, 1968 LUT4s, 4 EBRs	125 MHz
Altera CycloneII, ep2c5f256c8	1996 Les, 4 M4K BRAMs	70 MHz
Altera StratixII, ep2s15f484c5	1925 ALUTs, 4 M4K BRAMs	100 MHz
Xilinx Spartan3E xc3s250e-4tq144	1724 LUTs, 2 BRAMs	77 MHz
Xilinx Virtex4 xc4vlx15-10sf363	1698 LUTs, 2 RAMB16 BRAMs	200 MHz

Table 1: SYN1588Clock_S IP core resource utilization for varying FPGA families.

1.3.1 IP Core Block Diagrams

The top unit of the IP core has all interface signals required to connected the IP core to either a IEEE 802.3 standard MII interface (as shown in figure 5) or to a GMII interface as shown in figure 6.

Other interface configurations and IP Cores supporting on-the-fly time stamping are available upon request. Please contact Oregano Systems for further details.

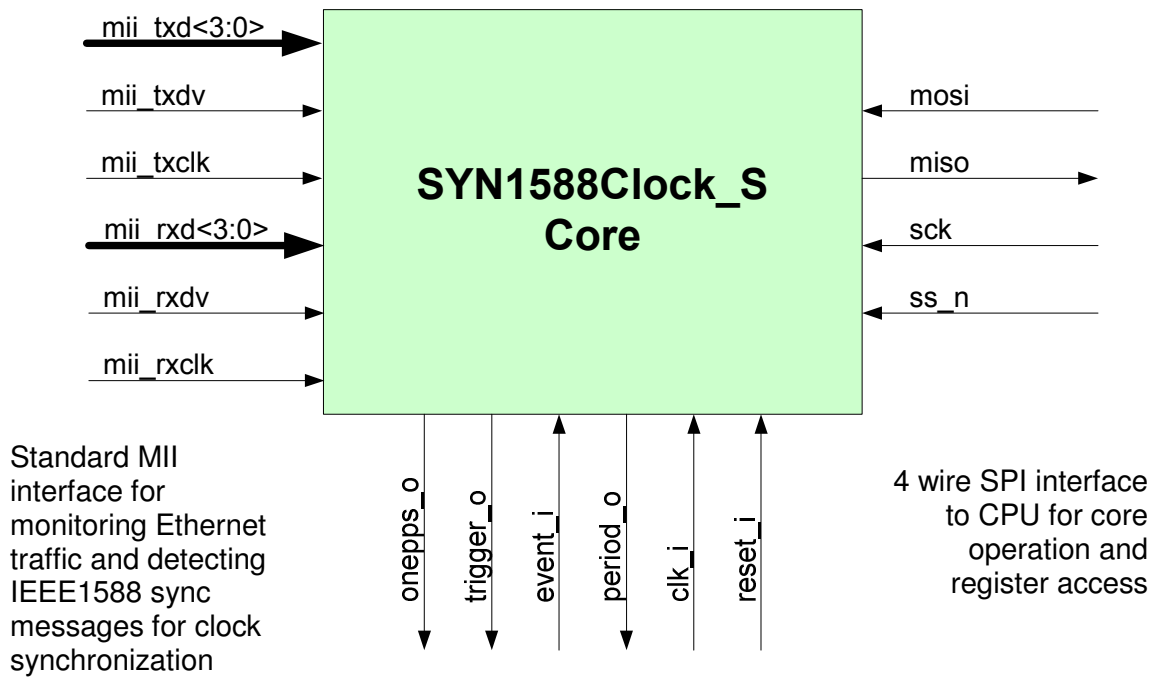


Figure 5: SYN1588Clock_S IP Core block diagram for 10/100 Mbps Ethernet.

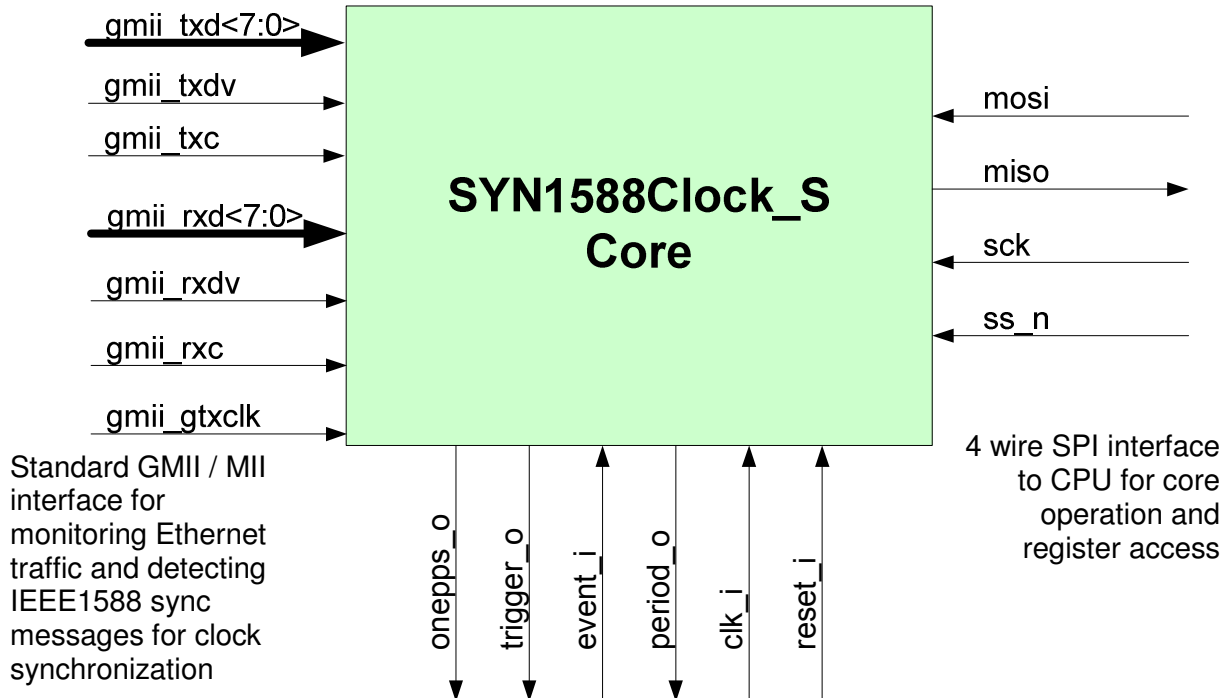


Figure 6: SYN1588Clock_S IP Core block diagram for 10/100/1000 Mbps Ethernet.

1.3.2 IP Core Interface Signal Description

Basic I/O Signals		
clk_i	Input	system clock
reset_i	Input	power up reset, asynchronous, active high
onepps_o	Output	one pulse per second output of clock (edge comes three system clock cycles + t_{co} after condition is true)
trigger_o	Output	clock dependent trigger output (edge comes two system clock cycles + t_{co} after condition is true)
event_i	Output	event input (has to be high for at least three system clock cycles)
period_o	Output	clock dependent periodical output (edge comes two system clock cycles + t_{co} after condition is true)
MII Interface		
mii_txclk	Input	MII transmit clock
mii_txdv	Input	MII transmit data valid
mii_txd<3:0>	Input	MII transmit data
mii_rxclk	Input	MII receive clock
mii_rxdv	Input	MII receive data valid
mii_rxd<3:0>	Input	MII receive data
SPI Interface		
sck_i	Input	SPI clock signal input
mosi_i	Input	SPI data input
miso_o	Output/HighImp.	SPI data output
ss_n_i	Input	SPI chip select

Table 2: SYN1588Clock_S IP core interface signals description for 10/100 Mbps Ethernet.

Basic I/O Signals		
clk_i	Input	system clock
reset_i	Input	power up reset, asynchronous, active high
onepps_o	Output	one pulse per second output of clock (edge comes three system clock cycles + t_{co} after condition is true)
trigger_o	Output	clock dependent trigger output (edge comes two system clock cycles + t_{co} after condition is true)
event_i	Output	event input (has to be high for at least three system clock cycles)
period_o	Output	clock dependent periodical output (edge comes two system clock cycles + t_{co} after condition is true)
GMII Interface		
gmii_txclk	Input	GMII transmit clock
gmii_txdv	Input	GMII transmit data valid

Basic I/O Signals		
gmii_txd<7:0>	Input	GMII transmit data
gmii_rxclk	Input	GMII receive clock
gmii_rxdv	Input	GMII receive data valid
gmii_rxd<7:0>	Input	GMII receive data
gmii_gtxclk	Input	Master clock from physical layer IC
SPI Interface		
sck_i	Input	SPI clock signal input
mosi_i	Input	SPI data input
miso_o	Output/HighImp.	SPI data output
ss_n_i	Input	SPI chip select

Table 3: SYN1588Clock_S IP core interface signals description for 10/100/1000 Mbps Ethernet.

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