Bringing Time in Line

syn1588® enabled IEEE 1588 compliant clock synchronisation

syn1588Clock_M IP Core

Brief Data Sheet

Version 1.5 – July 2nd 2010

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0. Legals

0.1 Version History

Version 1.5 July 2010

- Corrected block diagrams. Improved consistency of names throughout all syn1588® documents.

Version 1.4 June 2009

- GMII added

Version 1.3 Feburay 20th 2009

- Minor updates and type corrections

Version 1.2 March 10th 2008

- Major Update to include GMII and application data as well as V2. 0 support

Version 1.1 August 10th 2007

- Changed address of Oregano Systems

Version 1.0 September 28th 2006

- Initial release

0.2 Contents

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1. Overview

The syn1588®Clock_M IP-core provides highly accurate clock synchronization compliant to the IEEE1588 standard 2002 and 2008. It contains a high resolution, high accuracy hardware clock which uses a 96-bit wide adder based clock architecture allowing supporting input clock frequencies in the range of 10 – 200 MHz. Furthermore the syn1588®Clock_M comprises an MII-Scanner unit, which scans all Ethernet traffic in search for IEEE1588 synchronization packets. Upon detection of any such packet it draws a 80-bit wide time stamp from the local clock any copies it together with status and identification data into a so-called time-stamp FIFO.

2. Functional Description

In figure 1 the basic clock architecture used for all syn1588® IP cores is shown. The clock contains an accumulator whose increment and current value is user adjustable without causing glitches of spikes in the output signal.

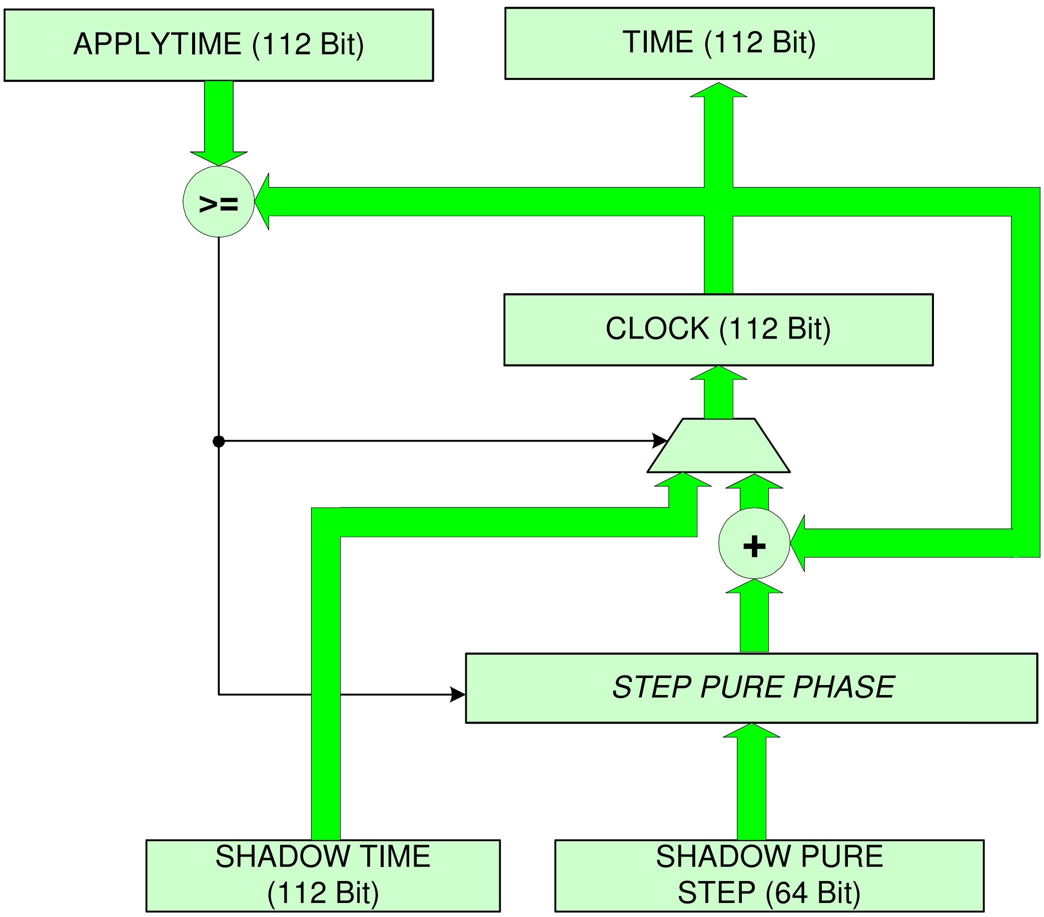

Figure 1: syn1588®Clock_M High Accuracy Clock Architecture.

The core is connected one of the system's Ethernet MII ports (according to IEEE 802.3 clause 22) and via a 32 bit wide AHB bus interface to a local CPU as show in figure 2.

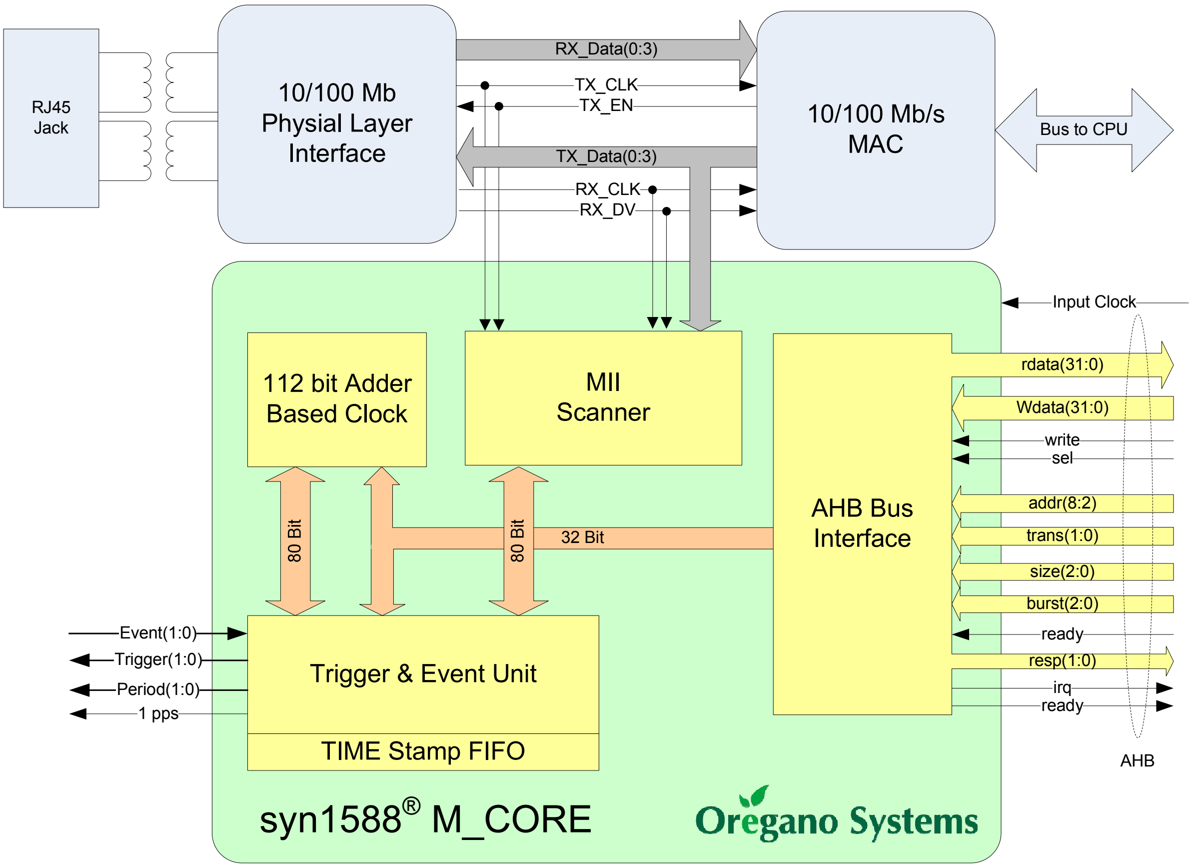

Figure 2: syn1588®Clock_M block diagram for MII

The core supports Gbit/s Ethernet transmission rates as well via the GMII interface (following IEEE 802.3u clause 22.4), to which is has to be attached for such a solution as shown in figure 2.

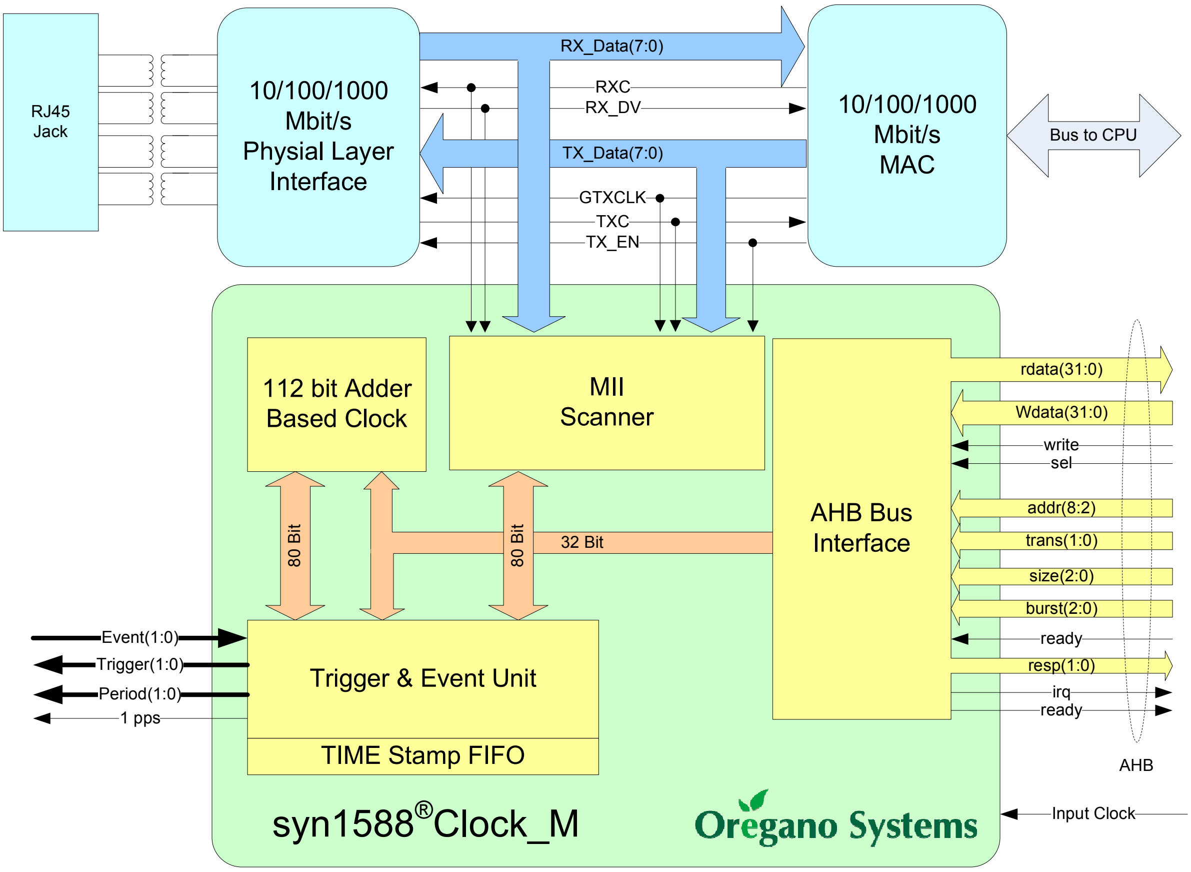

Figure 3: syn1588®Clock_M block diagram for GMII

The Oregano System's syn1588®Clock_M is intended to be integrated as a part of a larger FPGA design which may be attached to an external CPU as shown in Figure 4. This solution requires both a MAC IP-core and a bus controller interface e.g. a PCI-controller to be added to the design. Both these cells are available from Oregano Systems upon request as ready to use add-ons to the syn1588®Clock_M cell.

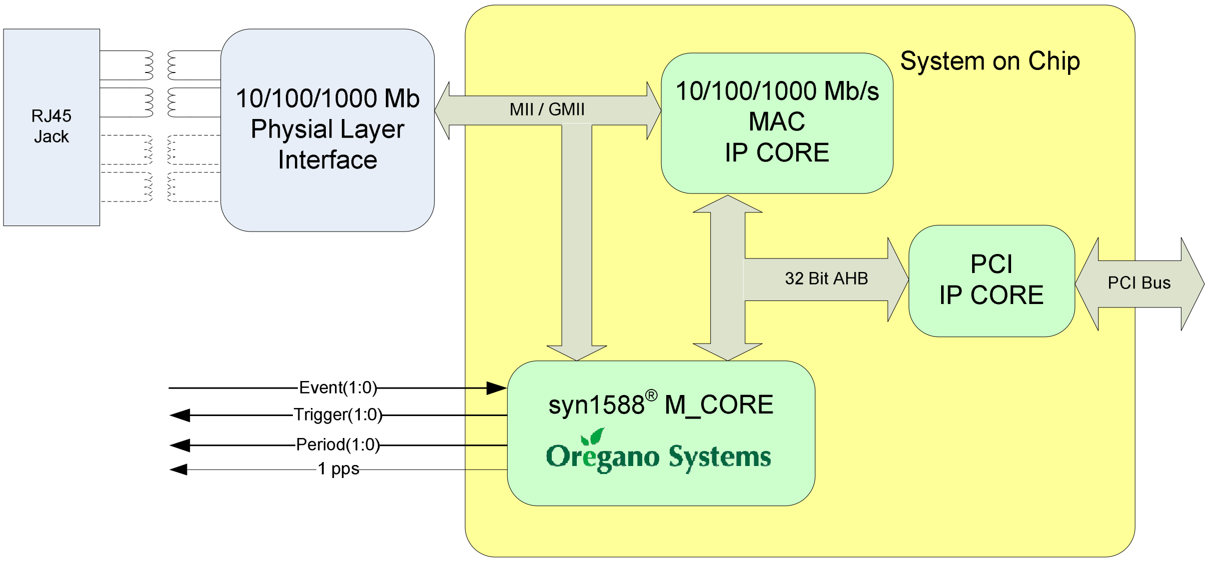

Figure 4: Block diagram of a typical Embedded System

Another system level option would be to build a complete SoC module capable of clock synchronization on its own and delivering synchronized time information by means of a 1pps signal or a phase locked frequency. Such a system is shown in figure 5, where an embedded CPU is used as a target CPU. Either an 8 bit 8051 like CPU or any one 32 bit CPU may be used.. As an example the 32 bit MICO32 core offered by LATTICE Semiconductor under GPL-like license conditions is suitable to run the drivers and the PTP-stack to operate as a fully functional IEEE1588 node. Please contact Oregano Systems for other bus interface and bus converters as shown in figure 5.

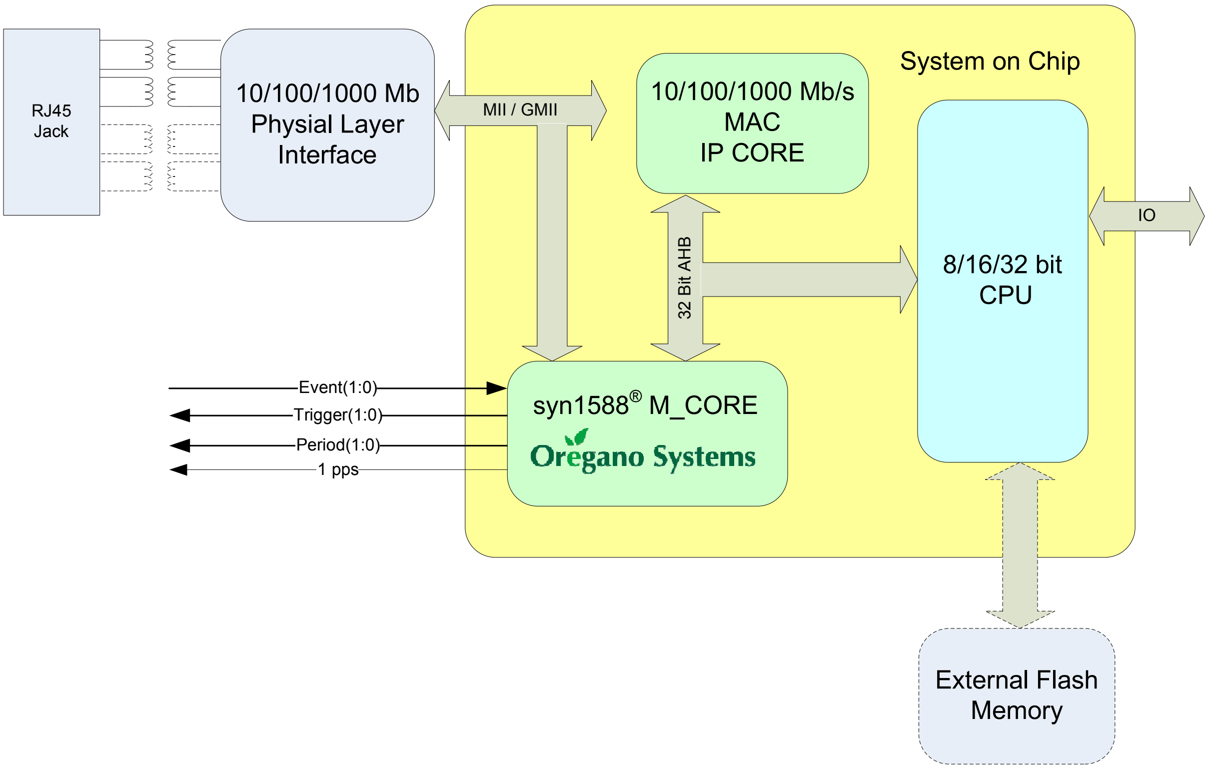

Figure 5: Block Diagram of a System on Chip

For layer 2 synchronization according to IEEE1588-2008 please contact Oregano Systems. There is also a solution available.

2.1 Features

Together with an appropriate IEEE 1588 compliant PTP-stack (also offered by Oregano Systems) the syn1588®Clock_M will synchronize its local clock to a master. A phase locked 1 pps pulse will be generated. If the syn1588®Clock_M IP core is connected to an external reference (e.g. a GPS based time source via a 1 pps input and a serial data line) the clock may lock to this pulse an act as a IEEE 1588 compliant master.

On application level the syn1588®Clock_M offers two so-called event-input pins, which may be used to record signal transitions with the accuracy of the syn1588® clock. Aside form the 1 pps output the IP core is able to generate two different arbitrary frequencies with a resolution of less than 0.1 Hz by means of two so-called period timers, which again are linked to the internal clock. Finally two trigger outputs allow to generate signal transition at given points in time.

The features of the IP core are summarized as follows:

- Seamless integration in SoCs
- The core is completely synchronous to the system clock
- All registers of the core operate with the rising edge of the system clock
- The clock time format is compatible to the IEEE1588 standard (2002 & 2008)
- Supports 10/100 Mbit/s half & full duplex modes via MII
- Supports 1000 Mbit/s full duplex mode via GMII
- 32-bit fully compliant AHB-Bus Interface operating at more than 100 MHz
- 1 pps output
- 2 period timer outputs allowing generating user configurable output frequencies with a period ranging from 14,000 sec down to 100 nsec with a resolution of 1 Hz.
- 2 event inputs which draw a time stamp and store it in the time stamp FIFO upon polarity changes of the input pin. Such an input may be used to synchronize to an external GPS-based time source via a 1 pps signal
- Events may be processed at a burst rate of 5 MHz. The sustained event rate processing capabilities are dependent on the performance of the host processor.
- 2 trigger output signals which may be used to generate a signal transition at a given point in time.
- All event, period, and trigger signals are strictly synchronous to the internal high accuracy clock.
- Enhanced MII scanners to be used to detect and subsequently time stamp a configurable type of Ethernet traffic both for send and receive data
- The time of the clock core is easily available via register accesses to the application software and so are the event, trigger, and period registers.
- Coded in VHDL in a fully synchronous way
- Delivered with test bench, 100% code coverage guaranteed
- Silicon proven

Optional features available upon request

- syn1588®PTP Stack for IEEE1588 version 1.0 and version 2.0 (Linux or Windows®)
- RMII interface support
- Other bus-interfaces and wrappers
- On-the-Fly time stamping in transmit direction to realize one-step clocks
- Interfaces to serializers/deserializers required to connect a Gbps physical layer IC to the MAC physical layer IC depending on the options of the hard wired IP cores of the respective target FPGA or ASIC technology
- Support of GPS timing receivers if one input is connected to the external 1 pps impulse from the receiver, given that the system provide the appropriate RS-232 connection all drivers are available upon request.

2.2 Resource Utilization

The following table designates the resource utilization of an implementation of several of the most common FPGA families and devices. If you need further information on resource utilization for a specific FPGA not listed please contact Oregano Systems.

For high accuracy and high speed applications Oregano Systems strongly recommends utilizing Xilinx devices.

Technology	Area	Frequency
Lattice XP lfxp20cfpbga484-3	2866 LUTs, 2 BRAMs	75 MHz
Altera Cyclone II, ep2c5f256c8	3386 Les,4 M4K BRAMs	70 MHz
Altera Stratix II, ep2s15f484c5	2402 ALUTs, 4 M4K BRAMs	125 MHz
Xilinx Spartan 3E xc3s250e-4tq144	2534 LUTs, 2 BRAMs	66 MHz
Xilinx Virtex 4, xc4vlx15-10sf363	2475 LUTs, 2 RAMB16 BRAMs	200 MHz

Table 1: syn1588®Clock_M IP core resource utilization for varying FPGA families.

For evaluation and licensing terms contact: www.oregano.at

2.3 Block Diagrams

The top unit of the IP core has all interface signals required to connected the IP core to either a IEEE 802.3 standard MII interface (as shown in figure 6) or to a GMII interface as shown in figure 7.

Other interface configurations and IP Cores supporting on-the-fly time stamping are available upon request. Please contact Oregano Systems for further details.

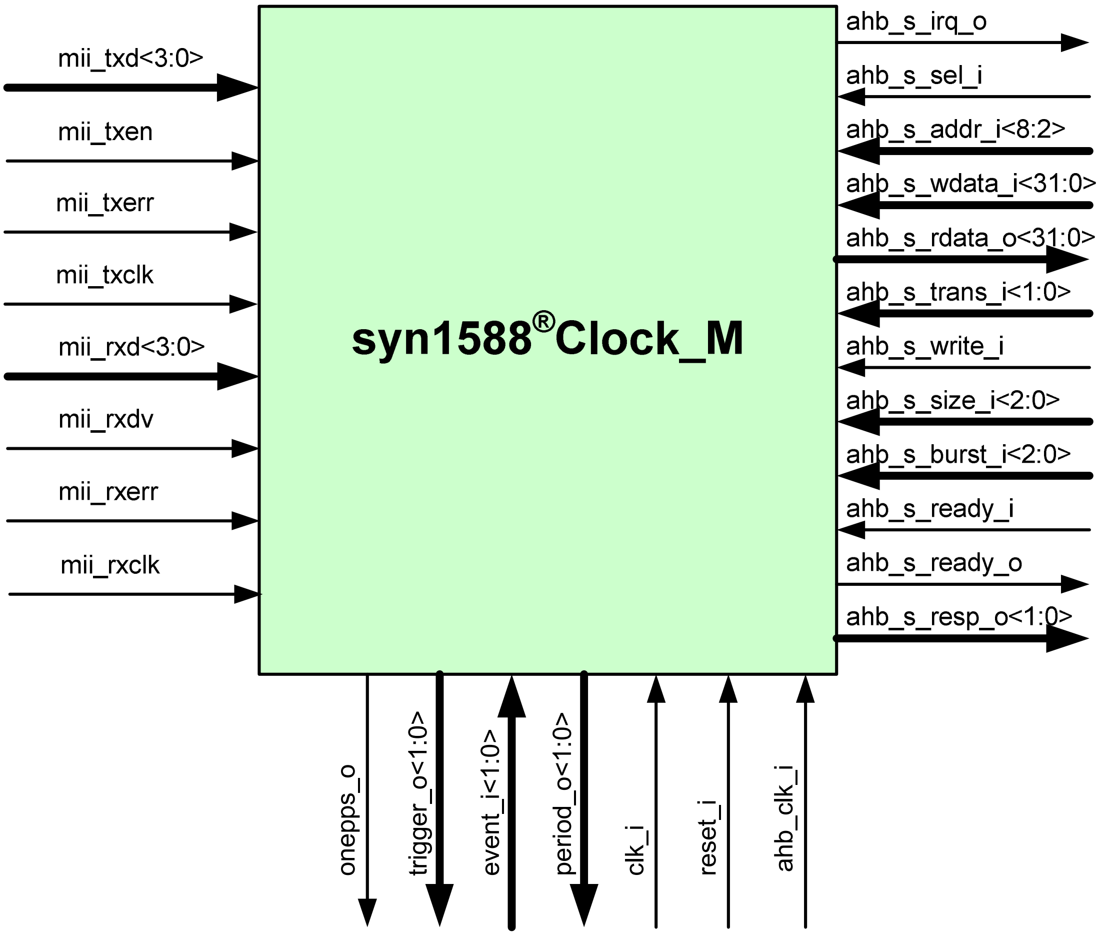

Figure 6: syn1588®Clock_M block diagram for 10/100 Mbps Ethernet.

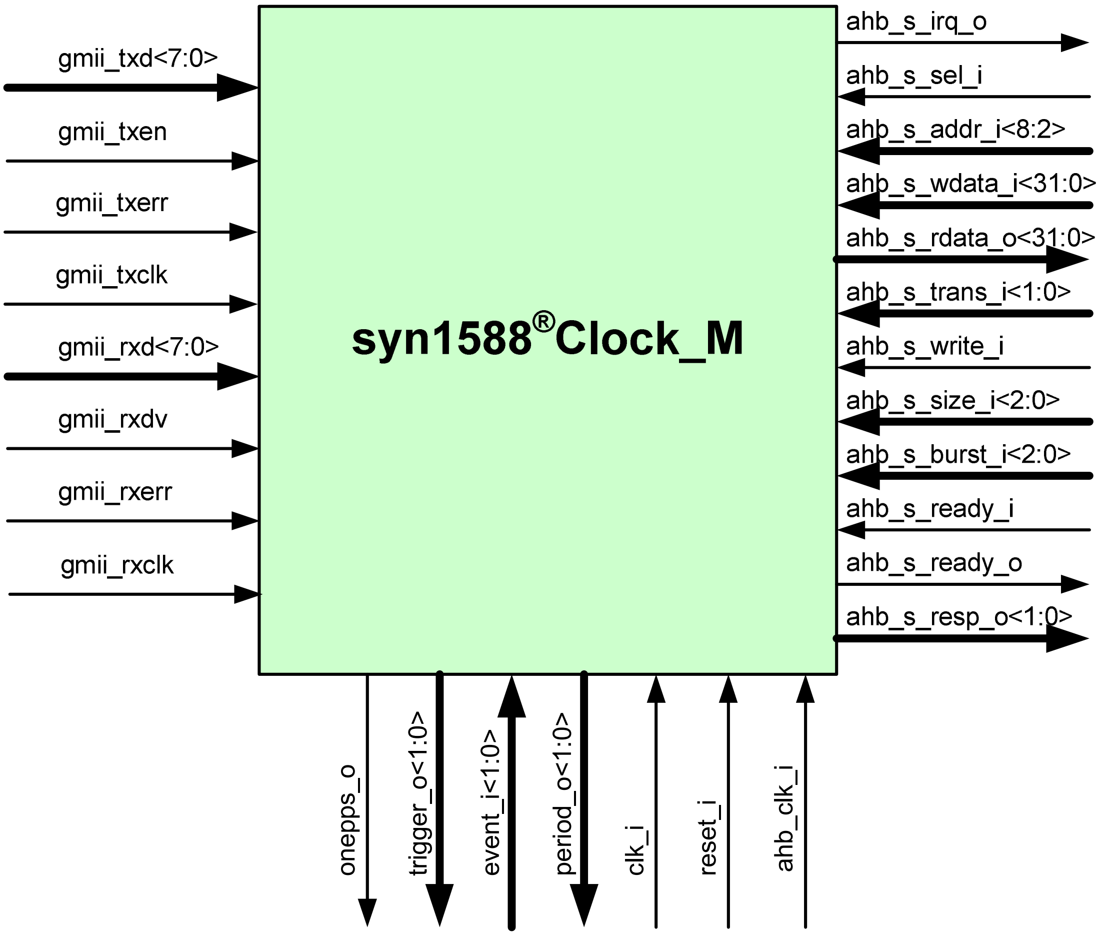

Figure 7: syn1588®Clock_M block diagram for 10/100/1000 Mbps Ethernet.

2.4 Interface Signal Description

The following table summarizes all interface signals of the IP core. Please note the MII and the GMII interface signals are mutually exclusive.

Basic I/O Signals		
clk_i	Input	system clock (precision clock)
ahb_clk_i	Input	AHB interface clock
reset_i	Input	power up reset, asynchronous, active high
onepps_o	Output	one pulse per second output of clock (edge comes three system clock cycles + t_{co} after condition is true)
trigger_o<1:0>	Output	two independent clock-dependent trigger outputs (edge comes two system clock cycles + t_{co} after condition is true)
event_i<1:0>	Iutput	two independent event inputs (has to be high for at least three system clock cycles)
period_o<1:0>	Output	two independent clock-dependent periodical output (edge comes two system clock cycles + t_{co} after condition is true)
AHB Slave Interface		
ahb_s_irq_o	Output	AHB slave interrupt signal
ahb_s_sel_i	Input	AHB slave chip select
ahb_s_addr_i<8:2>	Input	AHB slave address bus (word addresses only)
ahb_s_wdata_i<31:0>	Input	AHB slave write data bus
ahb_s_rdata_o<31:0>	Output	AHB slave read data bus
ahb_s_trans_i<1:0>	Input	AHB slave transaction flag
ahb_s_write_i	Input	AHB slave write signal
ahb_s_size_i<2:0>	Input	AHB slave byte enables
ahb_s_burst_i<2:0>	Input	AHB slave burst sequence
ahb_s_ready_i	Input	AHB slave ready input
ahb_s_ready_o	Output	AHB slave ready output
ahb_s_resp_o<1:0>	Output	AHB slave response signal
MII Interface		
mii_txclk	Input	MII transmit clock
mii_txen	Input	MII transmit data valid
mii_txerr	Input	MII transmit error
mii_txd<3:0>	Input	MII transmit data
mii_rxclk	Input	MII receive clock

mii_rxdv	Input	MII receive data valid
mii_rxerr	Input	MII receive error
mii_rxd<3:0>	Input	MII receive data
GMII Interface		
gmii_txclk	Input	GMII transmit clock
gmii_txen	Input	GMII transmit data valid
gmii_txerr	Input	GMII transmit error
gmii_txd<7:0>	Input	GMII transmit data
gmii_rxclk	Input	GMII receive clock
gmii_rxdv	Input	GMII receive data valid
gmii_rxerr	Input	GMII receive error
gmii_rxd<7:0>	Input	GMII receive data
gmii_gtxclk	Input	GMII transmit clock

Table 2: syn1588®Clock_M interface signals description (10/100/1000 Mbps Ethernet mode).